High-Speed Information Processing

UTAH STATE UNIVERSITY

CENTER

The purpose of this center (CHIP) is to design, prototype, and commercialize fast algorithm technologies for specific families of high-speed integrated circuit (IC) chips. When implemented in IC chips, fast algorithms such as these add great value to chip designers, chip manufacturers, and original equipment manufacturers (OEM) because their products are cheaper, faster, smaller, and less power hungry than those with standard algorithms that use multipliers and large amounts of memory. The use of our technologies offers additional benefits through faster design cycles, compact imple-

TECHNOLOGY

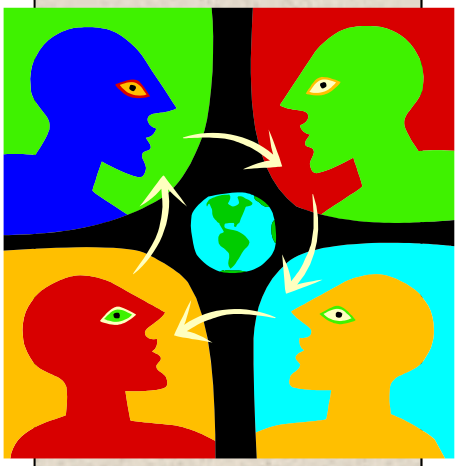
The center holds rights to several technologies such as: multiplier-free digital filters: design methodology and architecture; multiplier-free algorithms for hyperspectral image restoration and compression.; full-duplex echo canceller: algorithm and architecture; feedback cancellation algorithms for hearing aids.; Fast Integer Fourier Transform (FIFT).

ACCOMPLISHMENTS

This is the first year of funding for this Center. During this year multiplier-free algorithms for hyperspectral image restoration and compression was completed, a patent filed on full-duplex echo canceller and a patent filed on multiplier-free digital filter design. In CHIP, we have developed a full-duplex echo canceller using advanced signal processing. The new echo canceller enables natural, face-to-face like conversations with speaker phones and never cuts off or enters half-duplex mode. We have implemented the new echo canceller on a digital signal processing (DSP) chip that could be put into speaker phones for the home or office.

THINK TANK

What if there was...



A way to have face-to-face like conversations with a speaker phone without those annoying echos and cut offs???

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